IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the present application:

1-3 (Canceled).

4. (Original) A microprocessor comprising:

a first core;

a second core;

a first register to communicate information from the first core to the second core, wherein the first register is decoded by the first core to have a first register name and is decoded by the second core to have a second register name; and

a second register to communicate information from the second core to the first core, wherein the second register is decoded by the first core to have the second register name and decoded by the second core to have the first register name.

5. (Original) A microprocessor as recited in claim 4, wherein the first register is to communicate information only from the first core to the second core, and the second register is to communicate information only from the second core to the first core.

6. (Original) A microprocessor as recited in claim 4, wherein the first and second registers each include a bit used to synchronize operation of the first core and the second core.

7. (Original) A multi-thread microprocessor comprising:

a core to execute a first thread concurrently with a second thread;

a first register to communicate information from the first thread to the second thread, wherein the first register is decoded by the first thread to have a first register name and is decoded by the second thread to have a second register name; and

a second register to communicate information from the second thread to the first thread, wherein the second register is decoded by the first thread to have the second register name and decoded by the second thread to have the first register name.

8. (Original) A microprocessor as recited in claim 7, wherein the first register is to communicate information only from the first thread to the second thread, and the second register is to communicate information only from the second thread to the first thread.

9. (Original) A microprocessor as recited in claim 7, wherein the first and second registers each include a bit used to synchronize operation of the first thread and the second thread.

10-12. (Canceled)

13. (Original) A computer system comprising:

a microprocessor, the microprocessor including

a first core,

a second core,

a first register to communicate information only from the first core to the second core, wherein the first register is decoded by the first core to have a first register name and is decoded by the second core to have a second register name,

a second register to communicate information only from the second core to the first core, wherein the second register is decoded by the first core to have the second register name and decoded by the second core to have the first register name,

and

a shared cache coupled to the first core and the second core;

a random access memory coupled to the microprocessor; and

a read-only memory coupled to the microprocessor and storing firmware for execution by the microprocessor.

14. (Original) A computer system as recited in claim 13, wherein the first register is to communicate information only from the first thread to the second thread, and the second register is to communicate information only from the second thread to the first thread.

15. (Original) A computer system as recited in claim 13, wherein the first and second registers each include a bit used to synchronize operation of the first core and the second core.

16-22. (Canceled)

23. (Currently amended) A multi-core microprocessor comprising:

a plurality of cores, each of the cores having associated therewith a ~~first~~ read-only register to enable the core to receive information relating to another core of the microprocessor and a ~~second~~ read-write register to enable the core to output information for use by another core of the microprocessor; and

a logic circuit to apply a logic operation to contents of the ~~second~~ read-write register of each of the cores and to store a result of the logic operation in the ~~first~~ read-only register of each of the cores.

24. (Canceled)

25. (Original) A microprocessor as recited in claim 23, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the cores.

26. (Original) A microprocessor as recited in claim 23, wherein the logic circuit is programmable to select the logic operation.

27. (Original) A microprocessor as recited in claim 26, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

28. (Currently amended) A multi-thread microprocessor comprising:

a core to execute a first thread concurrently with a second thread; and

a plurality of registers, including a ~~first~~ read-only register for each of the threads to enable the thread to receive information relating to another thread of the

microprocessor and a ~~second~~ read-write register for each of the threads to enable the thread to output information for use by another thread of the microprocessor; and

a logic circuit to apply a logic operation to contents of the ~~second~~ read-write register of each of the threads and to store a result of the logic operation in the ~~first~~ read-only register of each of the threads.

29. (Canceled)

30. (Original) A microprocessor as recited in claim 28, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the threads.

31. (Original) A microprocessor as recited in claim 28, wherein the logic circuit is programmable to select the logic operation.

32. (Original) A microprocessor as recited in claim 31, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

33. (Original) A multi-core microprocessor comprising:

a plurality of cores, each of the cores having associated therewith

a read-only register to enable the core to receive information relating to another core of the microprocessor, and

a read-write register to enable the core to output information for use by another core of the microprocessor; and

a logic circuit to apply a logic operation to contents of the read-write register of each of the cores and to store a result of the logic operation in the read-only register of each of the cores.

34. (Original) A microprocessor as recited in claim 33, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the cores.

35. (Original) A microprocessor as recited in claim 33, wherein the logic circuit is programmable to select the logic operation.

36. (Original) A microprocessor as recited in claim 35, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

37-40. (Canceled)

41. (Original) A computer system comprising:

a microprocessor including a plurality of cores, each of the cores having associated therewith

a read-only register to enable the core to receive information relating to another core of the microprocessor, and

a read-write register to enable the core to output information for use by another core of the microprocessor; and

a logic circuit to apply a logic operation to contents of the read-write register of each of the cores and to store a result of the logic operation in the read-only register of each of the cores, and

a random access memory coupled to the microprocessor; and

a read-only memory coupled to the microprocessor and storing firmware for execution by the microprocessor.

42. (Original) A computer system as recited in claim 41, wherein the logic circuit applies the logic operation in a bit-wise manner to said contents of the read-write register of each of the cores.

43. (Original) A computer system as recited in claim 41, wherein the logic circuit is programmable to select the logic operation.

44. (Original) A computer system as recited in claim 43, wherein the logic circuit comprises a register, the contents of which determine the logic operation in a bit-wise manner.

45-57. (Canceled)

58. (Currently amended) A microprocessor comprising:

a first core;

a second core;

a first register to communicate information only from the first core to the second core, wherein the first register includes a plurality of bits used to synchronize operation of the first core and the second core; and

a second register to communicate information only from the second core to the first core, wherein the second register includes a plurality of bits used to synchronize operation of the first core and the second core.

59. (Canceled)

60. (Currently amended) A microprocessor as recited in claim ~~59~~ 58, wherein the first register and the second register are cross-decoded by the first core and the second core.

61. (Original) A microprocessor as recited in claim 60, wherein:

the first core is configured to execute a predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the first register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the second register is set to a predetermined value before proceeding; and

the second core is configured to execute the predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the second register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the first register is set to a predetermined value before proceeding.

62. (Original) An apparatus comprising:

a first register to communicate information from a first processing entity of a microprocessor to a second processing entity of the microprocessor;

a second register to communicate information from the second processing entity to the first processing entity;

means for cross-decoding the first register and the second register between the first processing entity and the second processing entity.

means for causing the first processing entity to set a predetermined bit of a plurality of bits in the first register to a predetermined value;

means for causing the first processing entity to wait until a corresponding predetermined bit of the plurality of bits in the second register is set to a predetermined value before proceeding.

63. (Original) An apparatus as recited in claim 62, wherein the first and second processing entities are separate cores of the microprocessor.

64. (Original) An apparatus as recited in claim 62, wherein the first and second processing entities are separate threads of the microprocessor.

65. (Currently amended) A computer system comprising:

a microprocessor including

a first core;

a second core;

a first register to communicate information only from the first core to the second core, wherein the first register includes a plurality of bits used to synchronize operation of the first core and the second core; and

a second register to communicate information only from the second core to the first core, wherein the second register includes a plurality of bits used to synchronize operation of the first core and the second core;

and

a shared cache coupled to the first core and the second core;

a random access memory coupled to the microprocessor; and

a read-only memory coupled to the microprocessor and storing firmware for execution by the microprocessor.

66. (Canceled)

67. (Original) A computer system as recited in claim ~~66~~ 65, wherein the first register and the second register are cross-decoded by the first core and the second core.

68. (Original) A computer system as recited in claim 67, wherein:

the first core is configured to execute a predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the first register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the second register is set to a predetermined value before proceeding; and

the second core is configured to execute the predetermined synchronization instruction by setting a predetermined bit of the plurality of bits in the second register to a predetermined value and then waiting until a corresponding predetermined bit of the plurality of bits in the first register is set to a predetermined value before proceeding.